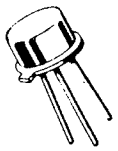
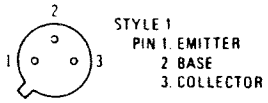
2N718A (SILICON)

2N718A JAN, JTX AVAILABLE
2N956
2N1711S





CASE 22
(TO-18)
2N718A
2N956

CASE 79
(TO-39)
2N1711

Collector connected to case

NPN silicon annular Star transistors for high-speed switching and DC to UHF amplifier applications.

*MAXIMUM RATINGS

Rating	Symbol	2N718A 2N956	2N1711	Unit
Collector-Emitter Voltage	V_{CER}	50		Vdc
Collector-Base Voltage	V_{CB}	75		Vdc
Emitter-Base Voltage	V_{EB}	7.0		Vdc
Total Device Dissipation @ T_A = 25°C	P_D	500	800	mW
Derate above 25°C		2.86	4.57	mW/°C
Total Device Dissipation @ T_C = 25°C	P_D	1.8	3.0	Watts
Derate above 25°C		10.3	17.1	mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

* Indicates JEDEC Registered Data

2N718A, 2N956, 2N1711S (continued)

***ELECTRICAL CHARACTERISTICS** (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Breakdown Voltage (I_C = 100 mAdc, pulsed; R_{BE} ≤ 10 ohms)		BV_{CER}	50	-	-	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)		BV_{CBO}	75	-	-	Vdc
Emitter-Base Breakdown Voltage (I_E = 100 μAdc, I_C = 0)		BV_{EBO}	7.0	-	-	Vdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0)		I_{CBO}	-	0.001	0.01	μAdc
(V_{CB} = 60 Vdc, I_E = 0, T_A = 150°C)			-	-	10	
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	2N718A, 2N956, 2N1711	I_{EBO}	-	-	0.010	μAdc
			-	-	0.005	
ON CHARACTERISTICS						
DC Current Gain (I_C = 0.01 mAdc, V_{CE} = 10 Vdc)	2N956, 2N1711	h_{FE}	20	-	-	-
(I_C = 0.1 mAdc, V_{CE} = 10 Vdc)	2N718A, 2N956, 2N1711		20	-	-	
			35	-	-	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)	2N718A, 2N956, 2N1711		35	-	-	
			75	-	-	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, T_A = -55°C)	2N718A, 2N956, 2N1711		20	-	-	
			35	-	-	
(I_C = 150 mAdc, V_{CE} = 10 Vdc)*	2N718A, 2N956, 2N1711		40	-	120	
			100	-	300	
(I_C = 500 mAdc, V_{CE} = 10 Vdc)*	2N718A, 2N956, 2N1711		20	-	-	
			40	-	-	
Collector-Emitter Saturation Voltage(1) (I_C = 150 mAdc, I_B = 15 mAdc)		$V_{CE(sat)}$	-	0.24	1.5	Vdc
Base-Emitter Saturation Voltage(1) (I_C = 150 mAdc, I_B = 15 mAdc)		$V_{BE(sat)}$	-	1.0	1.3	Vdc
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain—Bandwidth Product (I_C = 50 mAdc, V_{CE} = 10 Vdc, f = 20 MHz)	2N718A, 2N956, 2N1711	f_T	60	300	-	MHz
			70	300		
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)		C_{ob}	-	4.0	25	pF
Input Capacitance (V_{BE} = 0.5 Vdc, I_C = 0, f = 100 kHz)		C_{ib}	-	20	80	pF
Input Impedance (I_C = 1.0 mAdc, V_{CB} = 5.0 Vdc, f = 1.0 kHz)		h_{ib}	24	-	34	ohms
(I_C = 5.0 mAdc, V_{CB} = 10 Vdc, f = 1.0 kHz)			4.0	-	8.0	
Voltage Feedback Ratio (I_C = 1.0 mAdc, V_{CB} = 5.0 Vdc, f = 1.0 kHz)	2N718A, 2N956, 2N1711	h_{rb}	-	-	3.0	X 10^{-4}
			-	-	5.0	
(I_C = 5.0 mAdc, V_{CB} = 10 Vdc, f = 1.0 kHz)	2N718A, 2N956, 2N1711		-	-	3.0	
			-	-	5.0	
Small-Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	2N718A, 2N956, 2N1711	h_{fe}	30	-	100	-
			50	-	200	
(I_C = 5.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N718A, 2N956, 2N1711		35	-	150	
			70	-	300	
Output Admittance (I_C = 1.0 mAdc, V_{CB} = 5.0 Vdc, f = 1.0 kHz)		h_{ob}	0.1	-	0.5	μmho
(I_C = 5.0 mAdc, V_{CB} = 10 Vdc, f = 1.0 kHz)			0.1	-	1.0	
Noise Figure (I_C = 300 μAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N718A, 2N956, 2N1711	NF	-	-	12	dB
			-	-	8.0	

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

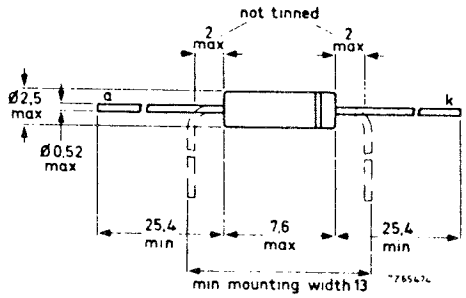
OA95

POINT CONTACT DIODE

Germanium diode in all-glass DO-7 envelope intended for general purposes.

MECHANICAL DATA

Dimensions in mm



The coloured band indicates the cathode

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Average reverse voltage (averaged over any 20 ms period)	V_R	max. 90	V
Repetitive peak reverse voltage	V_{RRM}	max. 115	V
Average forward current (averaged over any 20 ms period)	$I_{F(AV)}$	max. 50	mA
Repetitive peak forward current	I_{FRM}	max. 150	mA
Non-repetitive peak forward current (t < 1 s)	I_{FSM}	max. 500	mA
Storage temperature	T_{stg}	-55 to +75	°C
Ambient temperature	T_{amb}	-55 to +75	°C

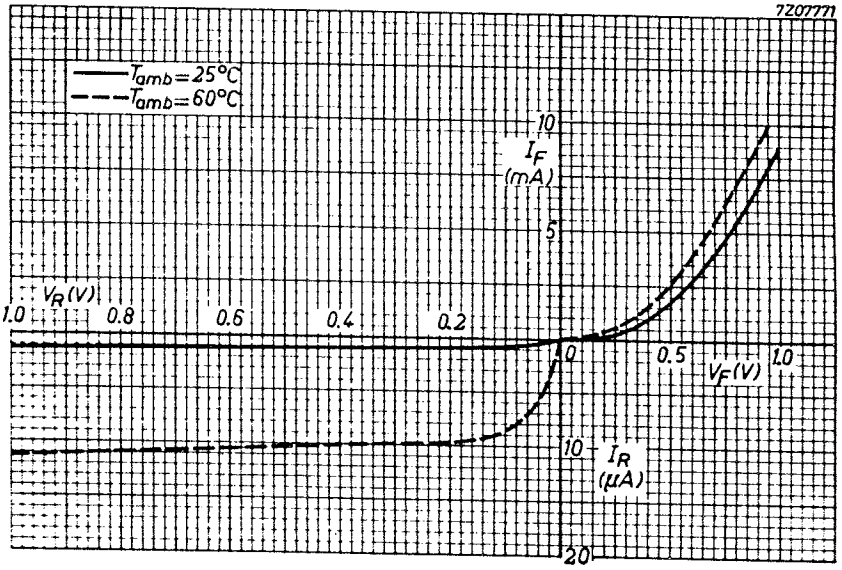
THERMAL RESISTANCE

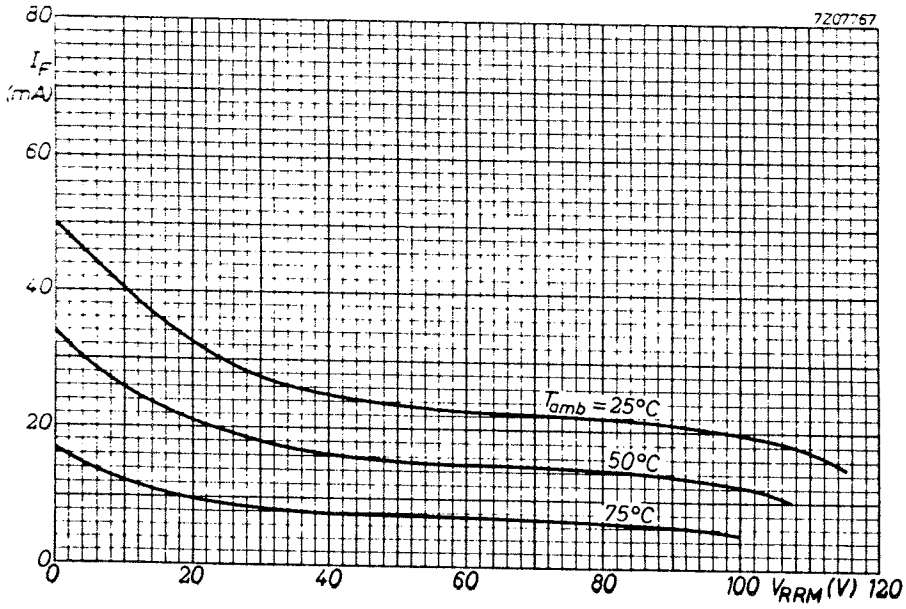
From junction to ambient in free air	$R_{th\ j\text{-}a}$	= 0.55 °C/mW

CHARACTERISTICS

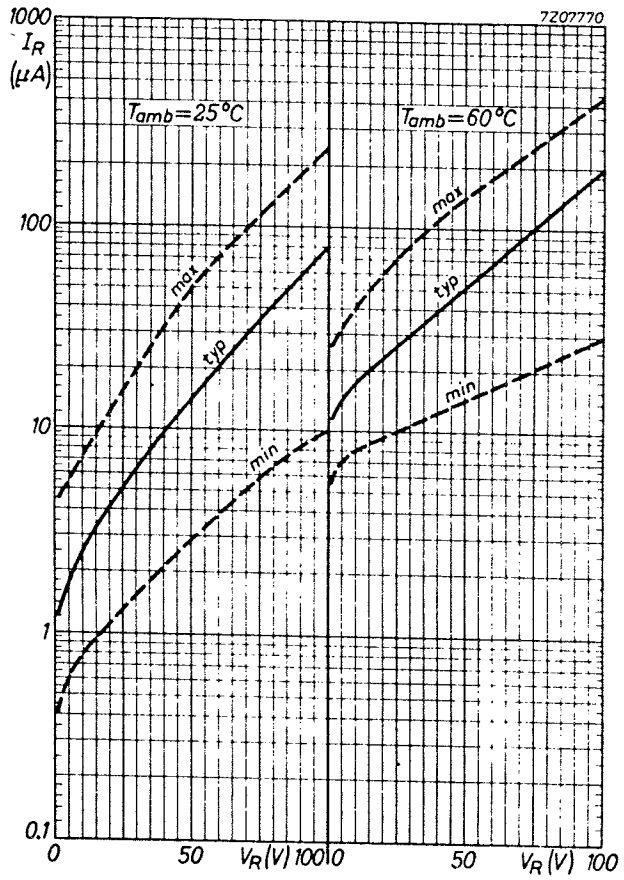
		T_{amb} = 25 °C	T_{amb} = 60 °C	
Forward voltage				
I_F = 0.1 mA	V_F	typ. 0.18	typ. 0.1	V
		0.1 to 0.25	0.05 to 0.2	V
I_F = 10 mA	V_F	typ. 1.05	typ. 0.95	V
		0.65 to 1.5	0.55 to 1.4	V
I_F = 30 mA	V_F	typ. 1.85	typ. 1.75	V
		1.0 to 2.6	0.9 to 2.5	V
Reverse current				
V_R = 1.5 V	I_R	typ. 1.2	typ. 12	µA
		0.4 to 4.5	5.5 to 26	µA
V_R = 10 V	I_R	typ. 2.5	typ. 17	µA
		0,8 to 7	8 to 40	µA
V_R = 75 V	I_R	typ. 35	typ. 100	µA
		5.7 to 110	20 to 250	µA
V_R = 100 V	I_R	typ. 80	typ. 200	µA
		10 to 250	30 to 430	µA

OA95





OA95



SCHOTTKY† PROMS

SERIES 24 AND 28 STANDARD, LOW-POWER, POWER-DOWN, REGISTERED PROGRAMMABLE READ-ONLY MEMORIES

BULLETIN NO. DL-S 12728, SEPTEMBER 1979

- New, Expanded Family of Standard, Low Power, Power Down, And Registered PROMs
- Titanium-Tungsten (Ti-W) Fuse Links for Reliable Low-Voltage Full-Family-Compatible Programming
- Full Decoding And Fast Chip Select Simplify System Design
- P-N-P Inputs for Reduced Loading On System Buffers/Drivers
- Each PROM Supplied With a High Logic Level Stored At Each Bit Location
- Applications Include:
  Microprogramming/Firm Ware Loaders
  Code Converters/Character Generators
  Translators/Emulators
  Address Mapping/Look-Up Tables

STANDARD PROMS

TYPE NUMBER		OUTPUT CONFIGURATION‡	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		
				ACCESS TIMES		POWER
NEW TYPE NUMBER	OLD TYPE NUMBER			ADDRESS	SELECT	DISSIPATION
TBP24S10 (J, N)†		▽	1024 Bits (256W X 4B)	35 ns	20 ns	375 mW
TBP24SA10 (J, N)†		◇				
TBP28S42 (J, N)†		▽	4096 Bits (512W X 8B)	35 ns	15 ns	500 mW
TBP28S45 (J, N)†		▽				
TBP24S41 (J, N)▲	SN74S476 (J, N)	▽	4096 Bits (1024W X 4B)	40 ns	20 ns	475 mW
TBP24SA41 (J, N)▲	SN74S477 (J, N)	◇				
TBP24S81 (J, N)	SN74S454 (J, N)	▽	8192 Bits (2048W X 4B)	45 ns	20 ns	625 mW
TBP24SA81 (J, N)	SN74S455 (J, N)	◇				
TBP28S86 (J, N)	SN74S478 (J, N)	▽	8192 Bits (1024W X 8B)	45 ns	20 ns	625 mW
TBP28SA86 (J, N)	SN74S479 (J, N)	◇				
TBP28S2708 (J, N)	SN74S2708 (J, N)	▽				
TBP28S85 (J, N)†		▽		35 ns	15 ns	550 mW
TBP28S166 (J, N)†		▽	16,384 Bits (2048W X 8B)	35 ns	15 ns	500 mW

LOW POWER PROMS

TYPE NUMBER		OUTPUT CONFIGURATION‡	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		
				ACCESS TIMES		POWER
NEW TYPE NUMBER	OLD TYPE NUMBER			ADDRESS	SELECT	DISSIPATION
TBP28L22 (J, N)†		▽	2048 Bits (256W X 8B)	45 ns	35 ns	300 mW
TBP28L42 (J, N)†		▽	4096 Bits (512W X 8B)	60 ns	30 ns	250 mW
TBP28L45 (J, N)†		▽				
TBP28L86 (J, N)▲	SN74LS478 (J, N)	▽	8192 Bits (1024W X 8B)	80 ns	35 ns	350 mW
TBP28L85 (J, N)†		▽		65 ns	30 ns	275 mW
TBP28L166 (J, N)†		▽	16,384 Bits (2048W X 8B)	65 ns	30 ns	250 mW

† NOTE – Electrical parameters for these devices are design goals only.

▲ NOTE – These devices available as full-temperature-range and as high-rel processed devices (use suffix MJ or NJ).

‡ ◇ = open collector, ▽ = three state.

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TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

SERIES 24 AND 28
STANDARD, LOW-POWER, POWER-DOWN, REGISTERED PROGRAMMABLE READ-ONLY MEMORIES

POWER DOWN PROMS

TYPE NUMBER		OUTPUT CONFIGURATION‡	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		
				ACCESS TIMES		POWER
NEW TYPE NUMBER	OLD TYPE NUMBER			ADDRESS	SELECT	DISSIPATION
TBP28P42 (J, N)†		▽	4096 Bits (5RW X 8B)	35 ns	35 ns	500/60 mW
TBP28P45 (J, N)†		▽				
TBP28P85 (J, N)†		▽	8291 Bits (1024W X 8B)	35 ns	35 ns	550.60 mW
TBP28P166 (J, N)†		▽	16,384 Bits (2048W X 8B)	35 ns	35 ns	500 75 mW

REGISTERED PROMS

TYPE NUMBER		OUTPUT CONFIGURATION‡	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		
				CLOCK TO	ADDRESS	POWER
NEW TYPE NUMBER	OLD TYPE NUMBER			OUTPUT	SET UP TIME	DISSIPATION
TBP 28R45 (J, N)†		▽	4096 Bits (512W X 8B)	20 ns	20 ns	550 mW
TBP28R85 (J, N)†		▽	8192 Bits (1024W X 8B)			600 mW
TBP28R166 (J, N)†		▽	16 384 Bits (2048W X 8B)			550 mW

† Electrical parameters for these devices are design goals only.
‡ ▽ = three state.

description

The new 24 and 28 Series of monolithic TTL programmable read-only memories (PROMs) feature an expanded selection of standard, low-power, power-down, and registered PROMs. This expanded PROM family provides the system designer with considerable flexibility in upgrading existing designs or optimizing new designs. Featuring proven titanium-tungsten (Ti-W) fuse links with low-current MOS-compatible pin-p inputs, all family members utilize a common programming technique designed to program each link with a 100-microsecond pulse.

The new 4096-bit and 8192-bit PROMs are offered in 24-pin 300-mil-wide packages, greatly improving system density for large PROM arrays. For systems requiring even higher levels of complexity and density, the 16,384-bit PROMs provide twice the bit density of the 8192-bit PROMs in 24-pin 600-mil-wide packages. All PROMs are supplied with a logic-high output level stored at each bit location. The programming procedure open-circuits Ti-W metal links, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs that have never been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

Active level(s) at the chip-select input(s) (S or $\overline{S}$) enables all of the outputs. An inactive level at any chip-select input causes all outputs to be off. On power-down PROMs, active level(s) at the chip-enable input(s) (E or $\overline{E}$) power up the device and enables all of the outputs. An inactive level at any chip-enable input causes all the outputs to be off and the PROM to be in a reduced-power standby mode.

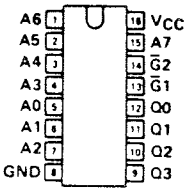
The three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus connected to other similar outputs, yet it retains the fast rise time characteristics of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull-up.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS TEXAS 75265

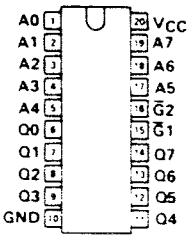
SERIES 24 AND 28
STANDARD, LOW-POWER, POWER-DOWN, REGISTERED PROGRAMMABLE READ-ONLY MEMORIES

PIN ASSIGNMENTS (TOP VIEWS)

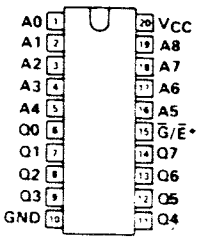
TBP24S10, TBP24SA10
1024 BITS
(256 WORDS BY 4 BITS)



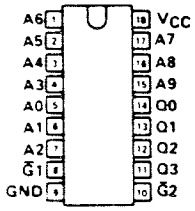
TBP28L22
2048 BITS
(256 WORDS BY 8 BITS)



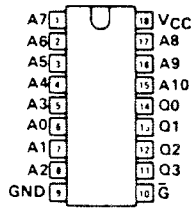
TBP28S42, TBP28L42,
TBP28P42* 4096 BITS
(512 WORDS BY 8 BITS)



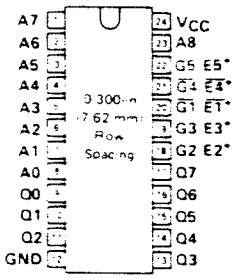
TBP24S41, TBP24SA41
4096 BITS
(1024 WORDS BY 4 BITS)



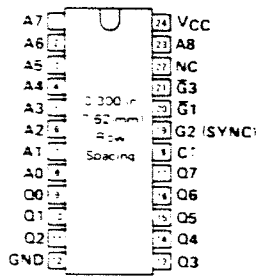
TBP24S81, TBP24SA81
8192 BITS
(2048 WORDS BY 4 BITS)



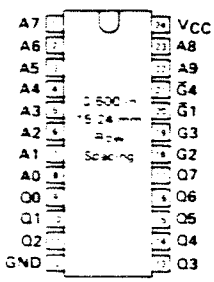
TBP28S45, TBP28L45, TBP28P45*
4096 BITS
(512 WORDS BY 8 BITS)



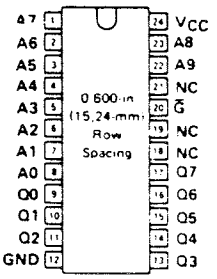
TBP28R45
4096 BITS
(512 WORDS BY 8 BITS)



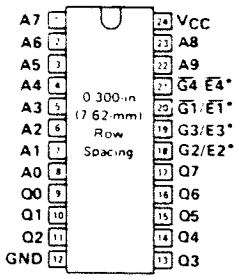
TBP28S86, TBP28SA86, TBP28L86
8192 BITS
(1024 WORDS BY 8 BITS)



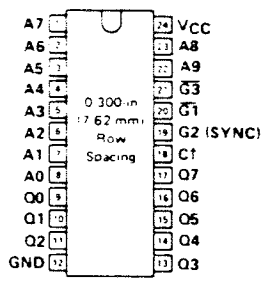
TBP28S2708
8192 BITS
(1024 WORDS BY 8 BITS)



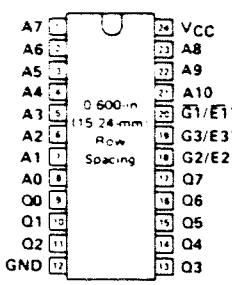
TBP28S85, TBP28L85, TBP28P85*
8192 BITS
(1024 WORDS BY 8 BITS)



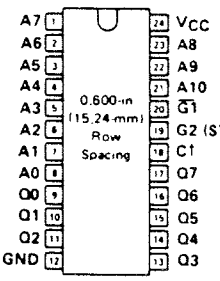
TBP28R85
8192 BITS
(1024 WORDS BY 8 BITS)



TBP28S166, TBP28L166, TBP28P166*
16,384 BITS
(2048 WORDS BY 8 BITS)



TBP28R166
16,384 BITS
(2048 WORDS BY 8 BITS)



NC = No internal connection

* For those pins having dual designations, the designation to the right of the virgule (/) applies only to the type number(s) immediately followed by an asterisk (*) above the pinout drawing.

Revised Nov. 79

For page 5 — 15

SERIES 24 AND 28
STANDARD, LOW-POWER, POWER-DOWN, REGISTERED PROGRAMMABLE READ-ONLY MEMORIES

standard PROMs

The standard PROM members of Series 24 and 28 offer the highest performance for applications requiring the uncompromised speed of Schottky technology. The fast chip-select access times allow additional decoding delays to occur without degrading speed performance.

low-power PROMs

To upgrade systems utilizing MOS EPROMs or MOS PROMs, the low-power PROM family offers the increased output drive and speed performance of bipolar technology and the reduced power dissipation necessary to implement effective upgrades. Additionally, low-power PROMs offer substantially reduced power dissipation over standard PROMs with minimal speed penalty.

power-down PROMs

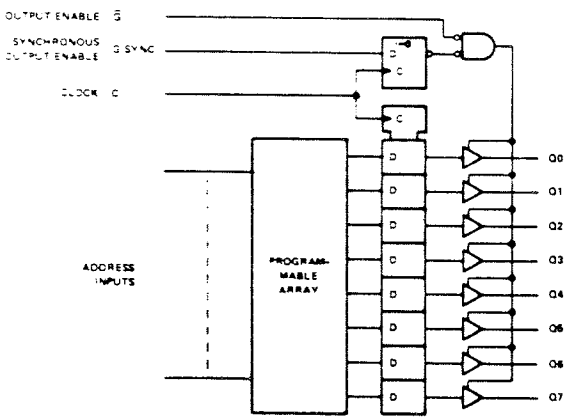
For power-sensitive systems requiring the speed performance of the standard PROM members as well as reduced system power dissipation, the power-down PROM members allow a 75% or better reduction in power dissipation when disabled while providing standard PROM speed performance when enabled. The power-down and power-up functions are sequenced to occur with the outputs at a high-impedance state. The enable (power-up) function provides adequate performance to allow power-up to occur during the normal read access time precluding any degradation in memory speed performance.

registered PROMs

For microprogrammed pipelined systems the Series 24 and 28 registered PROM members offer the system designer reduced package count and improved system performance by incorporating the pipeline register onto the PROM chip. Available in 4096-bit, 8192-bit and 16,384-bit densities, all registered PROMs are provided with synchronous and asynchronous output controls (G and $\overline{G}$) allowing maximum flexibility in data bus control.

When power is first applied, the edge-triggered latch for the synchronous output control is cleared, and the Q outputs are placed in a high-impedance state. To read data, the address is set up, the synchronous output enable, G(SYNC), is taken high, and a low-to-high transition on the clock (C) input causes the selected data to be stored in the registers. That same transition causes the outputs to be enabled if asynchronous output enable $\overline{G}$ is low. At this time the address may be changed and a new word addressed without affecting the register contents. If the synchronous output enable is low at the time of a low-to-high clock transition, the outputs will be disabled to the high-impedance state. They may be disabled at any time by taking output enable G high.

block diagram (positive logic)



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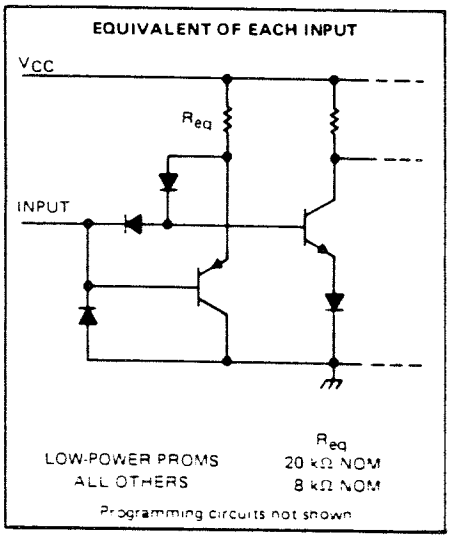
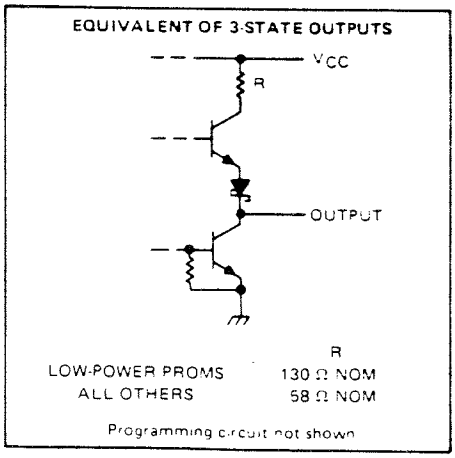
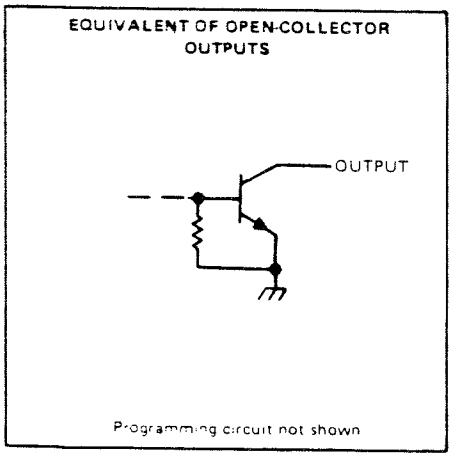
schematics of inputs and outputs







5

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)	7 V
Input voltage	5.5 V
Chip-select peak input voltage (S, S1, S2) (see Note 2)	11 V
Off-state output voltage	5.5 V
Off-state peak output voltage (see Note 2)	17.25 V
Operating free-air temperature range: Full-temperature-range circuits (MJ)	−55°C to 125°C
Commercial-temperature-range circuits (J, N)	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES 1. Voltage values are with respect to network ground terminal.
2. These ratings apply only under the conditions described in the programming procedure.